Properties of Latches/Flip-Flops

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EECS: 1100 Digital Logic Design
The University of Toledo

Lab Assignment #8

1. Objectives

- getting familiar with characteristic tables and characteristic functions of flip-flops,
- gaining experience in logic gate implementation of latches and flip-flops,
- gaining a close insight into the functioning and properties of basic static memory circuits,
- getting hands-on experience with the multiple toggling property of some flip-flops,
- getting hands on experience with the 1's catching property of some flip-flops,
- gaining insight into the static hazard property of combinational logic circuits,
- developing skills in the composition and testing of sequential logic circuits.

2. Prelab Assignment

2.1 THE NOR-LATCH

2.1.1 Prepare a computer generated drawing of a logic circuit of the NOR-latch and show it as Figure 2.1-1(a).

2.1.2 Design a physical layout of the logic circuit shown in Figure 2.1-1(a). Prepare a computer generated drawing of the layout and show it as Figure 2.1-1(b). Provide the IC package pinouts on both drawings of Figure 2.1-1.

Hint#1 Pinouts (pin numbers) are available in Figure 2.5 of the course text book, pp.107-109, and in the TTL Data Book.

2.1.3 Using only the present state variables R, S, and Q, prepare a *truth table* of the NOR-latch and show it as Table T2.1-1.

2.1.4 Simplify the truth table Table T2.1-1 by introducing the preceding stable state variable Q^-. Show the simplified truth table as table T2.1-2

Hint#2 Note that the table T2.1-1 should contain five rows, while the table T2.1-2 should contain one row less.

2.2 THE LEVEL CONTROLLED NOR-LATCH

2.2.1 Prepare a computer generated drawing of a logic circuit of the level-controlled RS-Latch and show it as Figure 2.2-1(a).

2.2.2 Using the collection of IC components listed in Section 3.2, design a physical layout of the logic circuit shown in Figure 2.2-1(a). Prepare a computer generated drawing of the layout and show it as Figure 2.2-1(b). Provide the IC package pinouts on both drawings of Figure 2.2-1.

2.2.3 Using the present stable state variables R, S, and Q, and the preceding stable state variable Q^-, prepare a *truth table* of the level-controlled RS-Latch and show it as Table T2.2-1. Compare the tables T2.1-2 and T2.2-1 and comment on their composition.

2.2.4 Using the prepared truth table T2.2-1 and the Karnaugh map minimization method, derive a minimized expression of the logic equation of the RS-Latch output variable Q. Show the derived equation as equation (2.2-1).

2.3 THE LEVEL CONTROLLED JK-FLIP-FLOP

2.3.1 Make the necessary additions to the logic circuit of Figure 2.2-1(a), which will convert the RS-Latch circuit into a level-controlled JK-flip-flop circuit; show the new circuit as Figure 2.3-1(a).

2.3.2 Using the collection of IC components listed in Section 3.2, design a physical layout of the JK-flip-flop logic circuit shown in Figure 2.3-1(a). Prepare a computer generated drawing of the layout and show it as Figure 2.3-1(b). Provide the IC package pinouts on both drawings of Figure 2.3-1.

Hint#3 Using the so far unused couple of AND gates of the IC 7408, create the necessary three-input AND gates by connecting two 2-input gates as a degenerate two-level 3-input AND circuit.

Hint#4 In anticipation of the assignment of Section 4.3.5, leave sufficient unused space at a convenient location on the protoboard to add two more ICs, one 7408 and one 7432, which will be needed for the construction of the logic circuit of Figure A.4-4.

2.3.3 Using the present state variables J, K, and Q, and the preceding state variable Q-, prepare a *truth table* of the level-controlled JK-flip-flop and show it as Table T2.3-1.

2.3.4 Using the prepared truth table T2.3-1 and the Karnaugh map minimization method, derive a minimized expression of the logic equation of the JK-flip-flop's output variable Q. Show the derived equation as equation (2.3-1)

3. Lab Equipment and Circuit Components

3.1 EQUIPMENT

Equipment to be used includes:

- Proto boards: Global PB-104, or PB-105,
- Agilent E3631A DC power supply,
- Function generator: Agilent 33120A,
- Mixed-Signal oscilloscope Agilent 54645D,
- Dell GxaEM computer system.

3.2 CIRCUIT COMPONENTS

- integrated circuit 7402, quad 2-input NOR gates (1)
- integrated circuit 7408, quad 2-input AND gates (2)
- integrated circuit 7432, quad 2-input OR gates (1)
- integrated circuit 7493, 4-bit ripple counter (1)

4. Lab Experiment

4.1 THE NOR-LATCH

4.1.1 Using as a reference the prepared physical layout diagram from Figure 2.1-1(b), build on the proto board the physical circuit that implements the NOR-latch. To test the circuit, add to the protoboard the auxiliary generator of all combinations of the input variables R and S. Figure A.4-1 shows the complete test circuit in which a pulse source (the function generator) and a binary counter serve as the generator of all combinations of the input variables.

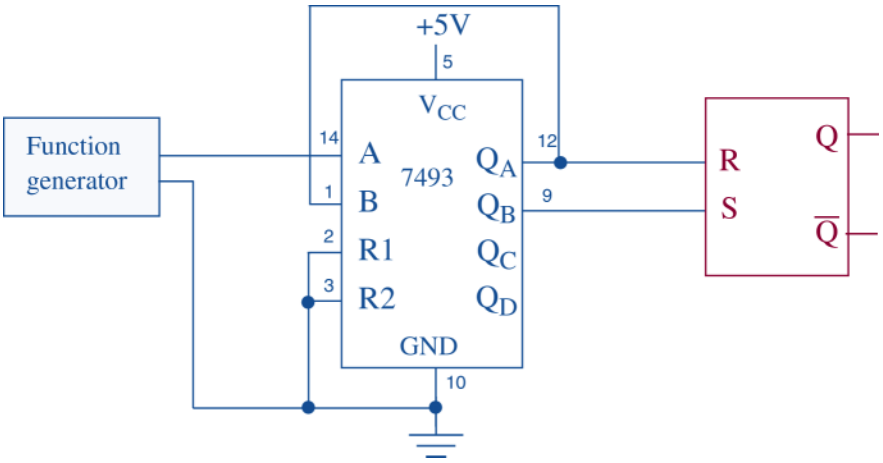

Figure A.4-1 The circuit for experimenting with the NOR-latch.

Hint#5 In anticipation of the work under the assignments 4.2 and 4.3, leave on the protoboard sufficient space for accommodating one 7408 IC between the IC 7493 and the NOR-latch circuit layout.

4.1.2 Connect the digital channels D0 through D4 of the Mixed-Signal oscilloscope Agilent 54645D to the circuit constructed under 4.1.1:

- digital channel D0: to the output of the Agilent 33120A function generator,
- digital channel D1: to the NOR-latch input R,
- digital channel D2: to the NOR-latch input S,
- digital channel D3: to the NOR-latch output Q,
- digital channel D4: to the NOR-latch output $\overline{Q}$.

Establish a ground connection. Turn on digital channels D0 through D4, and rename the channels D0 through D4 as A, R, S, Q and QB respectively.

4.1.3 To verify that the physical circuit has the correct placement of signal designations S, R, Q, and $\overline{Q}$, make the following temporary change to the circuit:

- remove the connection from Q_A to the input R, and remove the connection from Q B to the input S,
- connect the latch input R to ground, and the latch input S to +5V.

Hit the key *Single* on the Agilent 54645D and observe the I/O signal levels. Compare the observed signal levels with the contents of Table T2.1-1: the input S and the output Q should be at *logical 1* (High), while the input R and the output $\overline{Q}$ should be at *logical 0* (Low). Should it happen that the signal levels are not what they should be, explain the correction steps which would have to be made for both of the two feasible error conditions.

Hint#6 If your physical circuit has correct signal designations, it will help to first identify the two possible error conditions (S connected to ground, and R to +5V, or...?). Restore the circuit of Figure A-4.1.

4.1.4 Adjust the frequency of the Agilent 33120A function generator to 1MHz. Set the triggering mode of the Agilent 54645D to combination 00 on channels D1 through D2. Hit the key Single on the Agilent 54645D. Adjust the display of waveforms so that the first appearance of the combination of signal values 00 on channels D1 through D2 is positioned at the left end of the screen, and that the whole screen shows ten percent more than four periods of the signal at the input S.

4.1.5 Observe what happens to the outputs after the changes in logical values of the input signals (R and S in this case) from 11 to 00. Is the change in the outputs always the same? Repeat the experiment a few times if it happens to be the same.

4.1.6 Save the Screen Image of the correct waveforms of the channels D0 through D5 to a file named L8_416.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.2 LEVEL-CONTROLLED RS-FLIP-FLOP

4.2.1 Using as a reference the prepared physical circuit diagram of Figure 2-2(b), add to the already built NOR-latch circuit the two AND gates which will upgrade it to a level-controlled RS-flip-flop. Leave in place the auxiliary generator of all combinations of the input variables R and S. Connect the output Q_C of the 7493 counter to the Enable signal input of the RS-flip-flop. Figure A.4-2 shows the complete test circuit in which a pulse source (the function generator) and a binary counter serve as the generator of all combinations of the input variables.

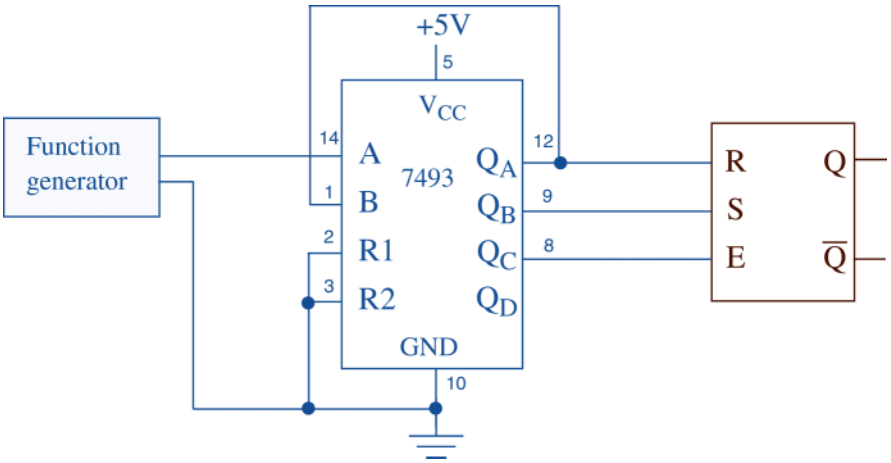

Figure A.4-2 The circuit for experimenting with the level controlled RS flip-flop.

4.2.2 Connect the digital channels D0 through D7 of the Mixed-Signal oscilloscope Agilent 54645D to the circuit constructed under 4.2.1:

- digital channel D0: to the output of the function generator,
- digital channel D1: to the flip-flop input signal R,
- digital channel D2: to the flip-flop input signal S,
- digital channel D3: to the flip-flop enable signal E,
- digital channel D4: to the NOR-latch input signal R,
- digital channel D5: to the NOR-latch input signal S.
- digital channel D6: to the NOR-latch output Q,
- digital channel D7: to the NOR-latch output $\overline{Q}$.

Establish a ground connection. Turn on digital channels D0 through D7, and rename the channels D0 through D7 as A, R, S, E, RL, SL, Q and QB respectively.

4.2.3 Adjust the frequency of the Agilent 33120A function generator to 1MHz. Set the triggering mode of the Agilent 54645D to combination 00 on channels D1 through D2. Hit the key Single on the Agilent 54645D. Adjust the display of waveforms so that the first appearance of the combination of signal values 00 on channels D1 through D2 is positioned at the left end of the screen, and that the whole screen shows ten percent more than two periods of the enable signal E.

4.2.4 Compare the obtained terminal waveforms of the RS flip-flop with those of the NOR-latch obtained under 4.1.4. What is the main difference? Could that difference be explained by the transparency control which is built into the flip-flop circuit?

4.2.5 Save the Screen Image of the correct waveforms of the channels D0 through D6 to a file named L8_425.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.3 EXPERIMENT WITH THE LEVEL-CONTROLLED JK-FLIP-FLOP

4.3.1 Using as a reference the prepared physical circuit diagram of Figure 2.3-1(b), transform the circuit of the level-controlled SR-flip-flop into a circuit of a level-controlled JK-flip-flop by adding two feedback connections from the outputs Q and $\overline{Q}$ to the third inputs of the AND gates. Leave in place the connections to the 7493; Figure A.4-3 shows the complete test circuit in which a pulse source (the function generator) and a binary counter serve as the generator of all combinations of the input variables.

4.3.2 Connect the digital channels D0 through D5 of the Mixed-Signal oscilloscope Agilent 54645D to the circuit constructed under 4.3.1:

- digital channel D0: to the output of the Agilent 33120A function generator,
- digital channel D1: to the flip-flop input signal J,
- digital channel D2: to the flip-flop input signal K,
- digital channel D3: to the flip-flop enable signal E,
- digital channel D4: to the flip-flop output Q,
- digital channel D5: to the flip-flop output $\overline{Q}$.

Establish a ground connection. Turn on digital channels D0 through D5, and rename the channels D0 through D5 as A, J, K, E, Q and QB respectively.

4.3.3 Repeat the actions of Section 4.2.3 on the JK-flip-flop. Compare the obtained terminal waveforms of the JK-flip-flop with those of the RS-flip-flop which were obtained under 4.2.3. What is the main difference? Could the difference be explained by the feedback which is built into the JK-flip-flop circuit?

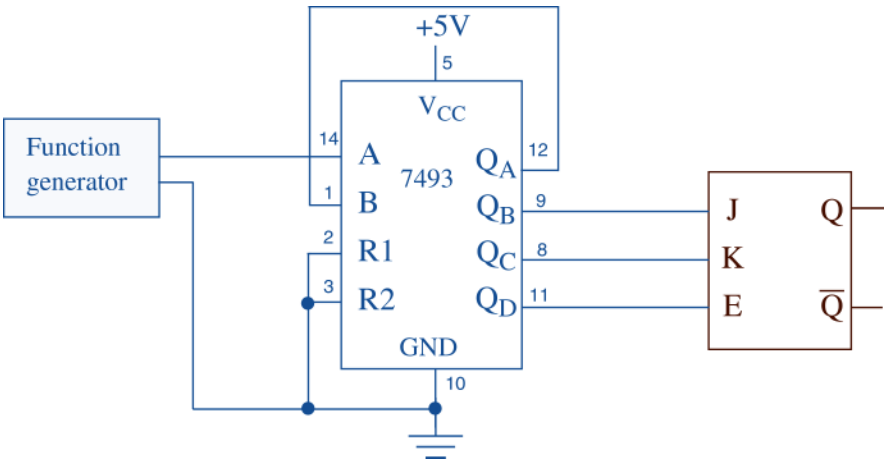

Figure A.4-3 The circuit for experimenting with the level-controlled JK-flip-flop.

4.3.4 Investigate the waveforms obtained under 4.3.3 looking for some evidence of errors caused by the *multiple toggling property*. At which input conditions may the multiple toggling occur? Can you observe it having had occurred? Based on your observations: Is the level-controlled JK-flip-flop a reliable memory element?

Save the Screen Image of the correct waveforms of the channels D0 through D5 to a file named L8_434.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.3.5 To demonstrate the 1's catching property of the level-controlled JK-flip-flop, add to the Circuit of Figure A.4-3 the NOR, AND, AND and OR gates, as shown in Figure A.4-4.

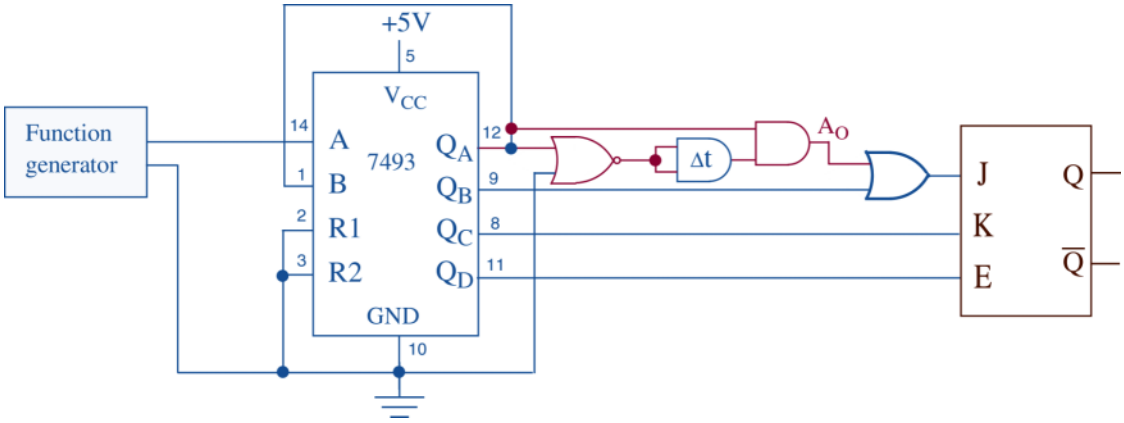

Figure A.4-4 A circuit which demonstrates the 1's catching property of the level-controlled JK-flip-flop.

Hint#7 Note that the NOR and AND gates in Figure A.4-4 create a combinational circuit with a static 0-hazard, which establishes conditions for the 1's catching to take place. To that effect, the static 0-hazard circuit will deliver a positive glitch to the input of the OR gate on every positive edge of the signal Q A; the glitch will be transferred to J input of the JK-flip-flop while Q B is at *logical 0*. The buffer-connected AND gate increases the time delay of the signal generated by the NOR gate to make the duration of the glitch longer.

4.3.6 Keep the logic channels D0 through D5 of the Agilent 54645D connected to the JK-flip-flop circuit as specified under 4.3.2. To monitor the correct operation of the static 0-hazard circuit, connect the channels D6 through D7 to the output A O of the 2-input AND gate and to Q A respectively, turn those two channels on and rename them to AO and Q A.

4.3.7 Repeat the experimental procedure of Section 4.2.3.

4.3.8 Investigate the waveforms obtained under 4.3.7 looking for the evidence of errors caused by the *multiple toggling* or *1's catching* properties of some flip-flop circuits. Could you observe any occurrences of those? Based on your observations: Is the level-controlled JK-flip-flop a reliable memory element?

Hint#8 To observe the 1's catching event it may be necessary to slightly adjust the frequency of the function generator, to avoid the situation in which the multiple toggling phase leaves the output in the state of logical 1.

4.3.9 Save the Screen Image of the correct waveforms of the digital channels D0 through D6 to a file named L8_439.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.4 TRANSFER OF CAPTURED WAVEFORMS.

Transfer (ftp) the files L8_*.tif from the Dell GxaEM computer system to your personal College of Engineering computer account.

5. Lab Report

To be considered complete, the lab report must contain the following,

1. Cover sheet - Lab style, filled out,
2. The truth tables prepared under 2.1 through 2.3.
3. The logic functions of flip-flop outputs derived under 2.2 and 2.3.
4. The logical and physical circuit diagrams prepared under 2.1 through 2.3.
5. The waveforms obtained in experiments 4.1 through 4.3.
6. Answers to all questions asked in conjunction with experiments 4.1 through 4.3.
7. A report on items not already included under 1. through 6. above, which includes:
   - a discussion of the insights gained through the conducted experiments,
   - textual description and graphical/ tabular illustration of the design procedure(s),
   - description of implemented testing procedures,
   - conclusions reached as a result of performing the lab experiment,
   - comments and suggestions that might lead to easier and/or deeper understanding of the topics covered by the assignment.